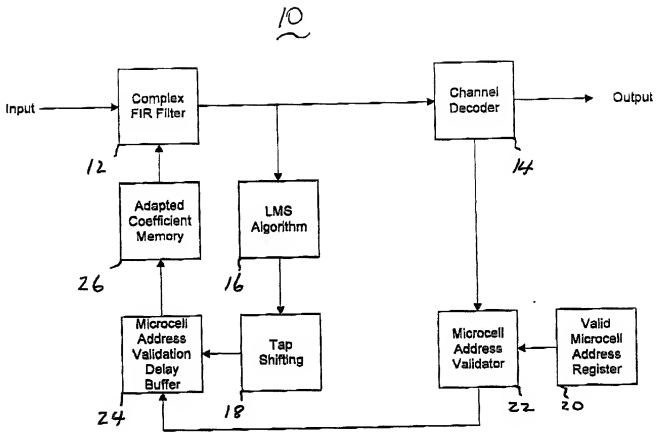
10
Input
Complex FIR Filter
12
Channel Decoder
14
Output
Adapted Coefficient Memory
26
LMS Algorithm
16
Microcell Address Validation Delay Buffer
24
Tap Shifting
18
Microcell Address Validator
22
Valid Microcell Address Register
20

FIG. 1

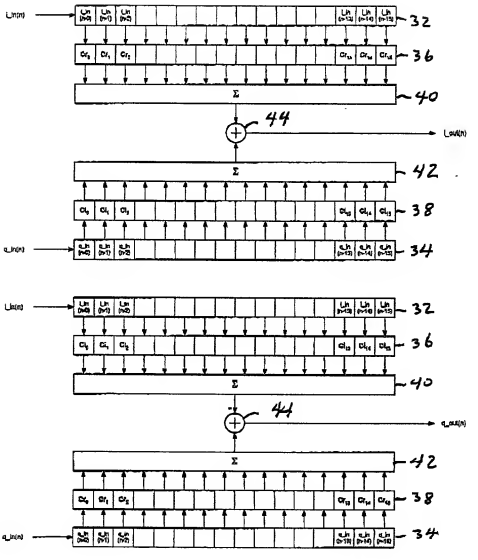
I_in(n)
32
36
Σ
40
44
I_out(n)
Σ
42
38
34
Q_in(n)
I_in(n)
32
36
Σ
40
44
Q_out(n)
Σ
42
38
34
Q_in(n)

FIG. 2

20070254002

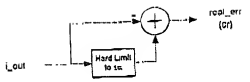

FIG. 3A

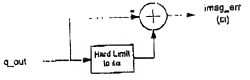

FIG. 3B

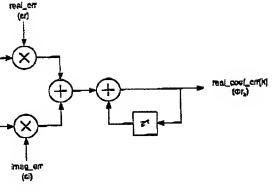

FIG. 4A

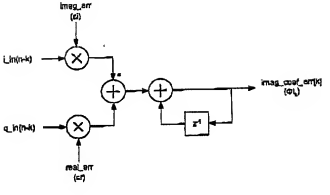

FIG. 4B

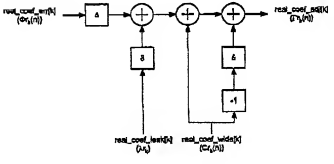

FIG. 5A

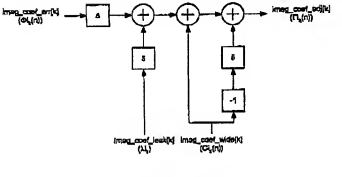

FIG. 5B

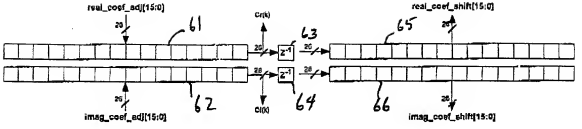

FIG. 6

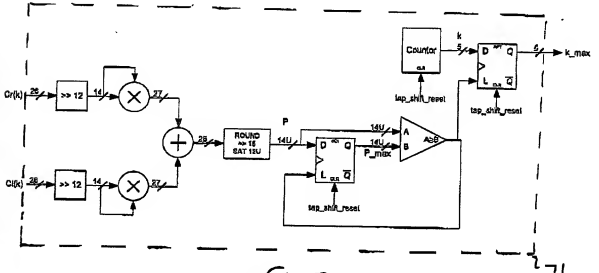

FIG. 7

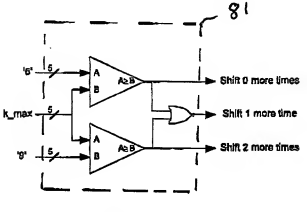

FIG. 8

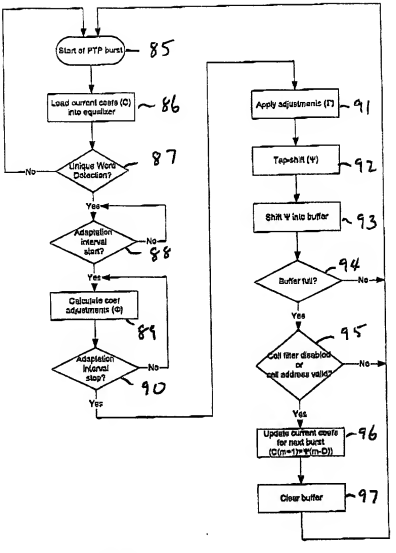

FIG. 9

Current Filter Coef	C0	C0	C0	C1	C1	C1	C4	C4	C4	C7	C7	C7	C11	C11	C11	C14
Cell Filter Buffer [0]	C1	C2	C3	C4	C5	C6	C7	C8	C9		C11	C12	C13	C14	C15	C16	C17
Cell Filter Buffer [1]	-	C1	C2	-	C4	C5	-	C7	C8	-		C11	C12	-	C14	C15	-
Cell Filter Buffer [2]	-	-	C1	-	-	C4	-	-	C7	-	-		C11	-	-	C14	-

FIG. 10

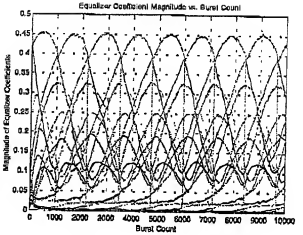
Equalizer Coefficient Magnitude vs. Burst Count
Magnitude of Equalizer Coefficients
Burst Count
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIG. 11

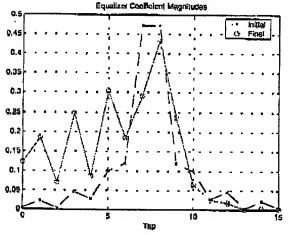
Equalizer Coefficient Magnitudes
Initial
Final
Tap
0
5
10
15

FIG. 12

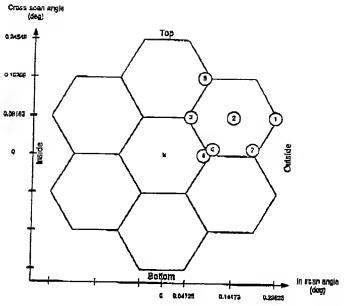

FIG. 13

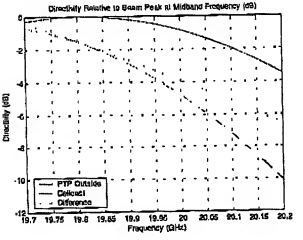

FIG. 14

13° Scan Angle	Degradation (dB)
With Microcell Address Validator	1.0
Without Microcell Address Validator	1.7

FIG. 15